What is claimed is:

1. A multi-queue network apparatus for quality of service oriented communication, comprising:

a host system comprising a system memory and a peripheral bus, the system memory including a plurality of queues each of which is configured to store data packets to be transmitted; and

a peripheral module comprising:

an arbiter, adapted to interface with the peripheral bus, maintaining a plurality of next access pointers targeting each queue within the system memory, respectively, determining which queue is to be serviced next contingent upon a quality of service policy, and fetching at least one data packet identified by the chosen queue's next access pointer;

a FIFO buffer, connected to the arbiter, storing and managing the fetched data packet in a first-in-first-out manner; and

physical layer interface logic, connected to the FIFO buffer, accepting therefrom each data packet, if available, and preparing the data packet for transmission on a physical medium.

2. The multi-queue network apparatus of claim 1 wherein the host system maintains a plurality of lists of descriptors targeting each queue within the system memory,

respectively, each list of descriptors includes access information for the data packets stored in an associated queue, and each descriptor is responsible for identifying one data packet.

3. The multi-queue network apparatus of claim 2 wherein each next access pointer points to the descriptor subsequent to a previous descriptor within a list of descriptors for a queue, in which the previous descriptor identifies the data packet most recently fetched from the queue.

4. A multi-queue network apparatus for quality of service oriented communication, comprising:

a host system comprising a system memory and a peripheral bus, the system memory including a plurality of queues each of which is configured to store data packets to be transmitted; and

a peripheral module comprising:

an arbiter, adapted to interface with the peripheral bus, maintaining a plurality of next access pointers targeting each queue within the system memory, respectively, determining which queue is to be serviced next contingent upon a quality of service policy, and fetching at least one data packet identified by the chosen queue's next access pointer;

a data path controller, connected to the arbiter, accepting therefrom the fetched data packet; and

two FIFO buffers, connected in parallel to the data path controller, storing and managing the fetched data packet in a first-in-first-out manner;

wherein the data path controller allows one of the FIFO buffers to be filled with the fetched data packet while the other FIFO buffer is engaged in outgoing transference.

5. The multi-queue network apparatus of claim 4 wherein the host system maintains a plurality of lists of descriptors targeting each queues within the system memory, respectively, each list of descriptors includes access information for the data packets stored in an associated queue, and each descriptor is responsible for identifying one data packet.

6. The multi-queue network apparatus of claim 5 wherein each next access pointer points to the descriptor subsequent to a previous descriptor within a list of descriptors for a queue, in which the previous descriptor identifies the data packet most recently fetched from the queue.

7. The multi-queue network apparatus of claim 4 wherein the peripheral module further comprises physical layer interface logic, connected to the two FIFO buffers, to prepare the data packet for transmission on a physical medium.

8. An apparatus for servicing multiple queues in a host system using reduced number of FIFO buffers, comprising:

an arbiter for maintaining a plurality of next access pointers for the multiple queues storing data packets to be transmitted, determining which queue is to be serviced next contingent upon a quality of service policy, and fetching at least one data packet, which is identified by the chosen queue's next access pointer, through a peripheral bus by means of direct memory access;

a FIFO buffer, connected to the arbiter, storing and managing the fetched data packet in a first-in-first-out manner; and

physical layer interface logic, connected to the FIFO buffer, accepting therefrom each data packet, if available, and preparing the data packet for transmission on a physical medium.

9. The apparatus of claim 8 wherein a plurality of lists of descriptors targeting each queue is maintained within a system memory of the host system, respectively, each list of descriptors includes access information for the data packets stored in an associated queue, and each descriptor is responsible for identifying one data packet.

10. The apparatus of claim 9 wherein each next access pointer points to the descriptor subsequent to a previous descriptor within a list of descriptors for an associated

queue, in which the previous descriptor identifies the data packet most recently fetched from the queue.